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Attorney Docket No.: 021230-000110US

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Washington, D.C. 20231

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MALACHY DEVLIN et al.

Application No.: Unassigned

Filed: Herewith

For: METHOD OF PROVIDING

POWER TO FIELD PROGRAMMABLE GATE

ARRAY MODULES

Examiner:

Unassigned

Art Unit:

Unassigned

INFORMATION

DISCLOSURE STATEMENT UNDER 37 CFR §1.97 and §1.98

**Assistant Commissioner for Patents** Washington, D.C. 20231

Sir:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the examiner. All of the references were cited in the parent application 10/076,883, filed February 13, 2002, and copies are not enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no

representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement, since it is being submitted prior to the first office action. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's deposit account number 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

Reg/No. 39,626

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Approved for use through 10/31/2002. OMB 0651-0031 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449B/PTO Complete if Known **Application Number** Unassigned INFORMATION DISCLOSURE **Filing Date** Herewith STATEMENT BY APPLICANT **First Named Inventor** Devlin, Malachy Group Art Unit Unassigned (use as many sheets as necessary) **Examiner Name** Unassigned Sheet of Attorney Docket Number 21230-000110US

		OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS	
Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
	0001	*EL7556BC Integrated Adjustable 6 Amp Synchronous Switcher,* Elantec Semiconductor, Inc. data sheet, August 30, 2000, pp. 1-13.	
	0002	Devlin, Malachy, et al., "DIME - The first module standard for FPGA based High Performance Computing," Proceedings of FPL'99, Glasgow, UK Sept. 1999, published as Springer LNCS 1673, 6 pages.	
	0003	*MAX4598 Low-Voltage, Combination Single-Ended 8-to-1/Differential 4-to-1 Multiplexer,* Maxim Integrated Products data sheet, October 1998, pp. 1-12.	
	0004	*DIME Module, Physical Level 0 Specification - Issue 4 NT301-0001,* Nallatech Ltd. data sheet, November 23, 2000, pp. 1-21.	
	0005	*Distributed DSP Processing, Level 1 Implementation of the DIME Module Standard NT301-0002,* Nallatech Ltd. data sheet, April 22, 1999, pp. 1-13.	
	0006	"Virtex™ -E 1.8 V Field Programmable Gate Arrays," Xilinx DS022 (v 1.2) Advance Product Specification, January 28, 2000, pp. 1-190.	
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Examiner	•	Date	
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<sup>&</sup>lt;sup>1</sup> Unique citation designation number. <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.